

## 7.5 Laboratory Procedure / Summary Sheet

Group: \_\_\_\_\_ Names: \_\_\_\_\_  
 \_\_\_\_\_

- (1) Using the datasheet pin-out diagrams (Figures 7.5 through 7.7), draw a complete and detailed wiring diagram (showing all connections and all pin numbers) for the circuit schematic shown in Figure 7.8, using a 7474 positive edge-triggered flip-flop. Carefully **label and number all pins that are used on each IC, including power and ground**. You might find Figure 7.9 helpful as a reference because it shows a photograph of a partially-completed circuit.

Be sure to **connect 5V and ground to both ICs** (otherwise, they won't function). **Also note that the 7474 has preset and clear features. Because these features are active low, these pins should be connected to 5V to deactivate them.**

**Note - It is good practice to include a 0.1  $\mu\text{F}$  capacitor across the power and ground pins of each IC (not shown in Figure 7.8 or Figure 7.9).** This helps filter out transients that could occur on the power and ground lines during switching. The capacitors are especially important in more complicated circuits where a single power supply may be providing reference voltages and switched current to numerous components.

**You will need to submit your detailed wiring diagram with your Lab summary and answered questions at the end of the Lab (see Question 4).**

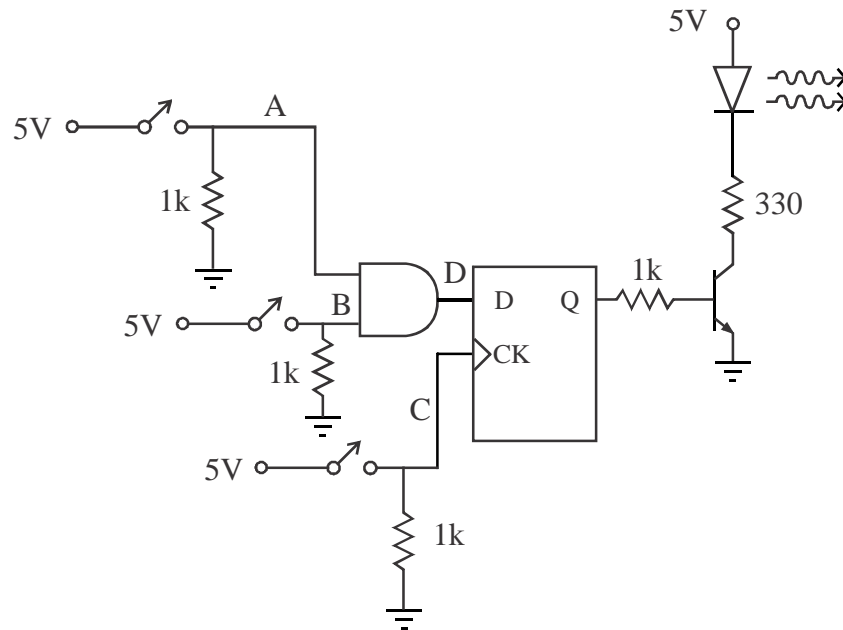


Figure 7.8 Circuit Schematic with Switches, Logic Gate, and Flip-flop

- (2) Using the detailed wiring diagram you created in Step 1, construct the circuit. Again, Figure 7.9 can be helpful as a reference because it shows the partially completed circuit; although, your main reference should be the wiring diagram you created in Step 1.

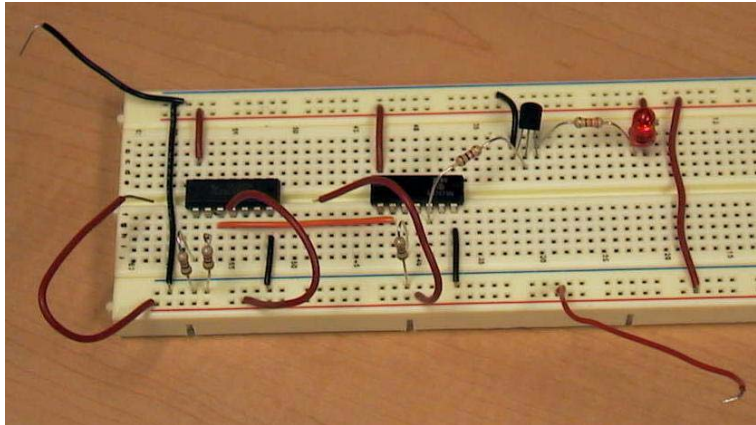


Figure 7.9 Photograph of the Partially-Completed Circuit

**NOTE - Don't use this photograph to build your circuit (because it is not complete). Instead, use the detailed wiring diagram you created in Step 1 above.**

- (3) Complete the following timing diagram (ignoring any switch bounce effects) and test the circuit to see if the results match the theory. **Have your TA verify that your circuit is working properly before continuing.** Also, look at and think about Question 2 at the end of the Lab before continuing.

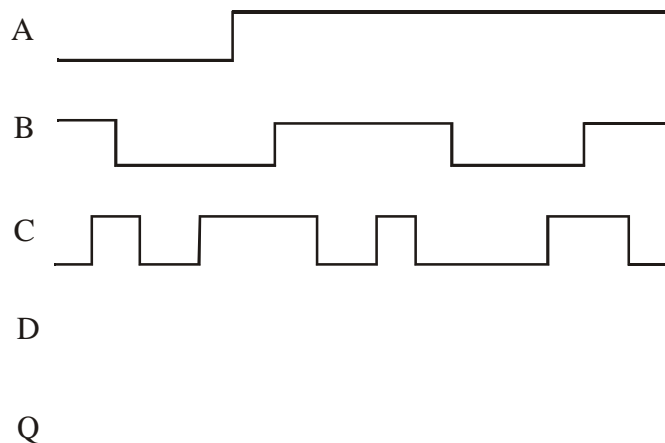


Figure 7.10 Positive-Edge-Triggered Circuit Timing Diagram

- (4) Replace the 7474 with the 7475 bistable data latch and rewire the circuit based on the circuit schematic in Figure 7.7. The circuit schematic is shown in Figure 7.11. The only difference from the previous circuit is that the D-latch is not edge triggered. Again, look at and think about Question 2 at the end of the Lab before continuing.

**NOTE - When removing ICs from a breadboard, always use a "chip puller" tool to lift both ends together. Alternatively, use a small flat-head screwdriver to pry each end up a little at a time to release the IC without causing damage (e.g., bent or broken pins).**

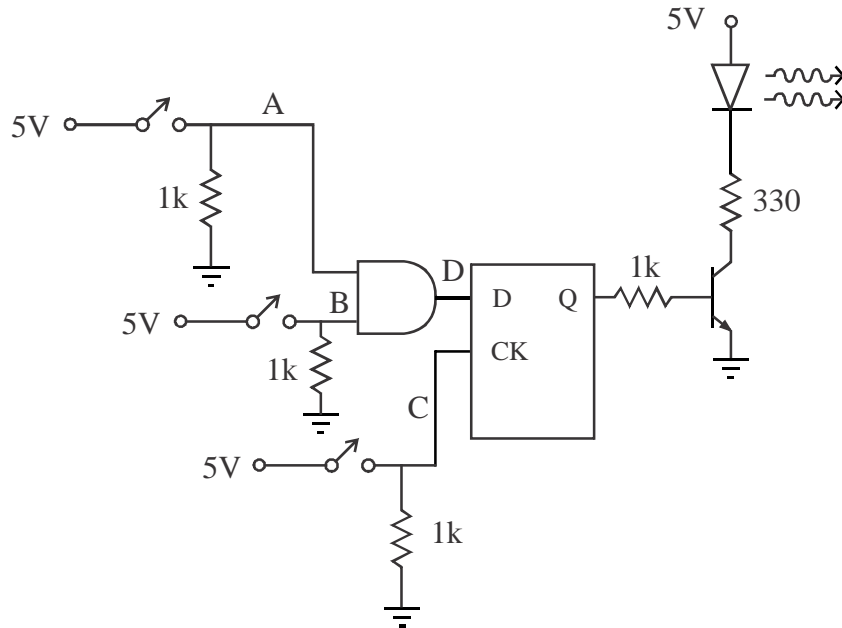


Figure 7.11 Data Latch Circuit Schematic

Complete the following timing diagram and verify the results by testing your circuit. **Have your TA verify that your circuit is working properly before continuing.**

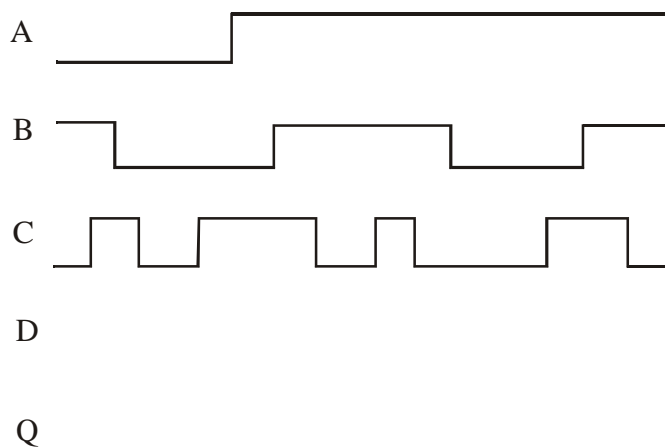


Figure 7.12 Latch Circuit Timing Diagram

**LAB 7 QUESTIONS**

Group: \_\_\_\_\_ Names: \_\_\_\_\_  
\_\_\_\_\_

- (1) Explain the difference between the output of the two circuits you analyzed and tested. What is the reason for the difference?
  
  
  
  
  
  
  
  
  
  
- (2) Switches and buttons often experience switch "bounce," especially when contact is made (as opposed to broken). Did bounce affect the output  $Q$  of the circuits? If so, in what cases, and why? If not, explain why you think this was the case.

For the positive-edge-triggered circuit (Figure 7.8), assuming bounce occurs during every release of button  $C$ , draw a timing diagram showing how the output ( $Q$ ) would respond for the  $A$ ,  $B$ , and  $C$  traces shown in Figure 7.10.

