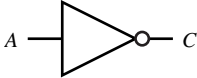
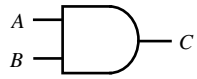
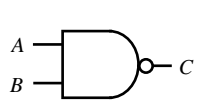

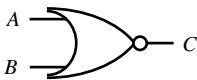
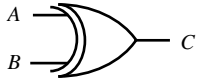
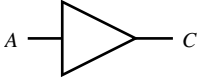


Table 6.3 Combinational logic operations

Gate	Operation	Symbol	Expression	Truth table															
Inverter (INV, NOT)	Invert signal (complement)		$C = \bar{A}$	<table border="1"> <tr><td>A</td><td>C</td></tr> <tr><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td></tr> </table>	A	C	0	1	1	0									
A	C																		
0	1																		
1	0																		
AND gate	AND logic		$C = A \cdot B$	<table border="1"> <tr><td>A</td><td>B</td><td>C</td></tr> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </table>	A	B	C	0	0	0	0	1	0	1	0	0	1	1	1
A	B	C																	
0	0	0																	
0	1	0																	
1	0	0																	
1	1	1																	
NAND gate	Inverted AND logic		$C = \overline{A \cdot B}$	<table border="1"> <tr><td>A</td><td>B</td><td>C</td></tr> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </table>	A	B	C	0	0	1	0	1	1	1	0	1	1	1	0
A	B	C																	
0	0	1																	
0	1	1																	
1	0	1																	
1	1	0																	
OR gate	OR logic		$C = A + B$	<table border="1"> <tr><td>A</td><td>B</td><td>C</td></tr> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </table>	A	B	C	0	0	0	0	1	1	1	0	1	1	1	1
A	B	C																	
0	0	0																	
0	1	1																	
1	0	1																	
1	1	1																	
NOR gate	Inverted OR logic		$C = \overline{A + B}$	<table border="1"> <tr><td>A</td><td>B</td><td>C</td></tr> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </table>	A	B	C	0	0	1	0	1	0	1	0	0	1	1	0
A	B	C																	
0	0	1																	
0	1	0																	
1	0	0																	
1	1	0																	
XOR gate	Exclusive OR logic		$C = A \oplus B$	<table border="1"> <tr><td>A</td><td>B</td><td>C</td></tr> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </table>	A	B	C	0	0	0	0	1	1	1	0	1	1	1	0
A	B	C																	
0	0	0																	
0	1	1																	
1	0	1																	
1	1	0																	
Buffer	Increase output signal current		$C = A$	<table border="1"> <tr><td>A</td><td>C</td></tr> <tr><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td></tr> </table>	A	C	0	0	1	1									
A	C																		
0	0																		
1	1																		